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| EXAMINER | |
|---|---|
| OLSEN, ALLAN W | |

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| 1716 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/599,106 | ZHU ET AL. | |
| | Examiner | Art Unit | |
| | ALLAN OLSEN | 1716 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 May 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-135* is/are pending in the application.

4a) Of the above claim(s) *34-135* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election of Group I, claims 1-33 in the reply filed on October 14, 2010 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)). Claims 34-135 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim.

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### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

**Claims 1, 10-14, 17, 22-24 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent 6,110,837 issued to Linliu et al. (hereinafter, Linliu).**

Regarding claim 1, Linliu teaches a method of fabricating a nanostructure array comprising: providing a substrate (figure 1, 100) having a top layer (figure 1, 120 or 130), and depositing a sacrificial layer having a first etching characteristic, patterning the sacrificial layer (figure 1, 200), forming a thin conformal layer (figure 2, 210) having a second etching characteristic over the patterned sacrificial structure, wherein the first and second etching characteristics are different, anisotropically etching the conformal layer to create a pattern (figure 3), removing the sacrificial layer (figure 4), transferring the resulting conformal layer structure to the substrate by etching, and removing any remaining conformal layer structure, thereby creating at least one nanostructure in the top layer (figure 7).

Regarding claim 10, Linliu teaches the substrate is a multilayer structure, comprising: a lower layer (100) comprising silicon, an intermediate layer (110) comprising an insulating material, an upper layer (120) comprising a semiconductor (see column 4, lines 12-18).

Regarding claim 11, Linliu teaches the intermediate insulating material is an oxide (see column 4, lines 12-18).

Regarding claim 12, Linliu teaches the upper semiconductor is polysilicon (see column 4, lines 12-18).

Regarding claim 13, Linliu teaches providing a protective layer (figures 1-8, 130 when layer 120 corresponds to the claimed layer) below the sacrificial layer.

Regarding claim 14, Linliu teaches the sacrificial layer is patterned by photolithography (column 4, lines 24-26).

Regarding claim 17, Linliu teaches the sacrificial layer is removed by wet etching (column 4, lines 62-63).

Regarding claims 22 and 23, Linliu teaches the substrate and the top layer comprise the same material (Si) and are separated by an insulator layer (see column 4, lines 12-18).

Regarding claim 24, by virtue of the photolithography process, Linliu teaches at least one nanostructure is fabricated on a predetermined location with positional control.

Regarding claim 30, Linliu teaches the nanostructure comprises the top layer of the substrate (figure 8).

**Claims 1-4 and 6-33 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent Application Publication 2004/0136866 as filed by Pontis et al. (hereinafter, Pontis).**

Regarding claim 1, Pontis teaches a method of fabricating a nanostructure array comprising: providing a substrate (figure 6A, 606) having a top layer (figure 6B, 608 or figure 6A, 602), and depositing a sacrificial layer having a first etching characteristic, patterning the sacrificial layer (figure 6E, 610), forming a thin conformal layer (figure 6F, 616) having a second etching characteristic over the patterned sacrificial structure, wherein the first and second etching characteristics are different, anisotropically etching the conformal layer to create a pattern (figure 6G, 618, 620), removing the sacrificial layer (figure 6H), transferring the resulting conformal layer structure to the substrate by

etching, and removing any remaining conformal layer structure, thereby creating at least one nanostructure in the top layer (figure 6J).

Regarding claims 2-4 and 6-9, Pontis teaches reducing the dimension of the nanostructure by thermal oxidation of Si nanowires and contacting with an etchant to remove the oxide ([0061]).

Regarding claims 10-12, Pontis teaches the substrate is a multilayer structure, comprising: a lower layer (606) comprising silicon, an intermediate layer (604) comprising an insulating material, such as an oxide, an upper layer (602) comprising a semiconductor, such as silicon (see [0073]).

Regarding claim 13, Pontis teaches providing a protective layer (608) below the sacrificial layer.

Regarding claim 14, Pontis teaches the sacrificial layer is patterned by photolithography ([0073]).

Regarding claim 15, Pontis teaches the conformal layer comprises silicon oxide ([0074]).

Regarding claim 16, Pontis teaches the conformal layer can be formed by chemical vapor deposition, spin coating, sputtering, evaporation or chemical reaction with the sacrificial layer ([0074]).

Regarding claim 17, Pontis teaches the sacrificial layer is removed by wet etching ([0077]).

Regarding claims 18-21, Pontis teaches forming a contact in intimate contact with at least one nanostructure wherein the contact is formed by forming a conducting film, photolithographically masking the contact area, and etching any exposed film away ([0080] - [0086], [0107])).

Regarding claims 22 and 23, Pontis teaches both the substrate and the top layer comprise the same material (Si) and they are separated by an insulator layer ([0073]). Regarding claim 24, by virtue of the photolithography process, Pontis teaches at least one nanostructure is fabricated on a predetermined location with positional control ([0050]).

Regarding claim 25, Pontis teaches there are between 1000 and 1 billion nanostructures on the array, which are fabricated on a predetermined location and with positional control ([0114]).

Regarding claims 26-29, Pontis teaches functionalizing different nanostructures with different functionalizing including agents such as one or more receptors selected from the group consisting of ss-DNAs, proteins, antibodies, platinum, photoactive molecules, photonic nanoparticle, inorganic ion, inorganic nanoparticle, magnetic ion, magnetic nanoparticle, electronic nanoparticle, metallic nanoparticle, metal oxide nanoparticle, gold nanoparticle, gold-coated nanoparticle, carbon nanotube, nanocrystal, quantum dot, protein domain, enzyme, hapten, antigen, biotin, digoxygenin, lectin, toxin, radioactive label, fluorophore, chromophore, or a chemiluminescent molecule ([0108] – [0111]).

Regarding claim 30, Pontis teaches the nanostructure comprises the top layer of the substrate (figure 6K).

Regarding claim 31, Pontis teaches at least one contact positioned on a top layer of the substrate, and the contact, the nanostructure and the top layer comprise the same material ([0086] with the sacrificial silicon layer corresponding to the claimed contact)

Regarding claim 32, Pontis teaches at least one contact is positioned in intimate contact with more than one nanostructure ([0113], multiplexing circuitry).

Regarding claim 33, Pontis teaches the nanostructure comprises a material selected from the group consisting of $SnO_2$, $TiO_2$. Fe oxides, ZnO, $WO_3$, $Ga_2O_3$ and perovskites ([0099]).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

**Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pontis as applied above to claim 3.**

Pontis does not teach using a controlled $XeF_2$ etch to the reduction a dimension of the nanostructure.

The examiner takes Official Notice that the use of $XeF_2$ to etch Si is well known and that it would be obvious to etch the Si with $XeF_2$ because this etching method is particularly noted for being an extremely clean process that is very controllable. See additional remarks below.

***Response to Arguments***

Applicant's arguments filed May 17, 2011 have been fully considered but they are not persuasive. With respect to the rejection of claims being anticipated by Linliu, applicant argues that Linliu fails to teach the limitation that requires transferring the conformal layer to create a pattern, removing the sacrificial layer, transferring the resulting conformal layer structure to the substrate by etching. Applicant states that in the structure taught by Linliu the substrate is identified by reference character 100. As noted by applicant, Linlui teaches a process wherein a conformal layer structure is

transferred into layers 120 and 130 but Linliu does not teach transferring the structure all the way down to the base layer 100. However, applicant's claims are directed to a process of fabricating a nanostructure in a substrate having a top layer and claim 1 explicitly recites that the nanostructure is transferred into the top layer of the substrate. The examiner maintains that the top layers 120 or 130 of Linliu correspond to the claimed top layer of the substrate; this is especially true in light of applicant's own definition of "substrate" on page 12 of their specification wherein it states:

> *"By "substrate" it is meant a layer or layers of materials on which the nanostructure array can be fabricated. The substrate may be a single layer of Si, preferably as pure as possible, preferably at least 99.9 % pure. The substrate may be transparent (as for use in an optoelectronic device) or opaque. Generally the thickness of the substrate, whether it is one or multiple layers, is between 500 nm and 1rmm, but this can vary depending on the intended use.*
>
> *Silicon is a preferred material for the substrate. However, also contemplated as materials include $SIO_2$, Group II-VI and Group III-V semiconductors, any glass or quartz, sapphire, polished metals providing they have an insulating coating. The wafer size may be any size depending on the manufacturing parameters. For the purpose of fabricating a functional device, it is to be understood that the substrate preferably has either have an insulator material thereon, or the substrate comprises an insulator, such as $SIO_2$, $A1_20_3$ or other insulating material. Oxides are preferred because they are capable of processing at high temperatures. The insulating layer may be grown, deposited by any CVD technique, sputtering or evaporation or ion implantation.*
>
> *By "SOI" it is meant "silicon on insulator". This is a substrate comprising multiple layers, that Si/insulator/Si. The top layer and bottom layer may be substituted for other materials as described herein, for the present invention."*

Regarding the rejection of claims 1-4 and 6-33 as being anticipated by Pontis, applicant adopts a differing view of the claimed substrate by emphasizing that the claim recites creating a nanostructure **in the top layer**. Applicant argues that the nanostructure created by Pontis, features 626 and 628 of figure 6L, are not created in the top layer because according to applicant the "top layer" of the Pontis substrate is nitride layer 608 as shown in figure 6B. If, on the other hand, one viewed the top layer of Pontis to be layer 602 as shown in figure 6A then the nanostructures 626 and 628 would indeed be formed in the top layer, Again, the examiner points to page 12 of applicant's specification wherein a SOI (silicon on insulator) structure s identified as one exemplary substrate. The examiner notes that figure 6A of Pontis depicts a SOI substrate having a top layer 602 from which the nanostructures are fabricated.

Regarding the rejection of claim 5 under 35 USC 103, as being unpatentable over Pontis, applicant challenges the examiner's reliance on Official Notice regarding the use of a $XeF_2$ controlled etch to reduce the size of a Si nanostructure. In accordance with MPEP 2144.03 C[1] the examiner herein provides documentary evidence in support of the Official Notice. XeF2 is a molecule that is notorious for its ability to etch silicon without even without the use of a plasma. The fact that XeF2 is very closely associated with the etching of silicon is demonstrated in part by the following data from a search of the US Patent and US PG-Pub data bases:

[1] If applicant adequately traverses the examiner's assertion of official notice, the examiner must provide documentary evidence in the next Office action if the rejection is to be maintained. See 37 CFR 1.104(c)(2). See also *Zurko*, 258 F.3d at 1386, 59 USPQ2d at 1697

a search of XeF2 yields 3,572 hits;

a search of XeF2 and silicon yields 3,082 hits (86%);

a search of XeF2 and silicon and etch yields 2,864 hits (80%).

The following references serve as examples from the above noted 2,864 hits:

US 20070117396: see [0041]

US 20090321644: see [0039], [0043], [0044], [0100] and [0118]

US 20110006208: see [0097]

US 4393127: see column 13, lines 13-17

US 6764898: see column 11, line 61 – column 12, line 5.

Additionally, the following exemplary citations from a Google search of "XeF2 silicon etch" provide further documentary evidence is in support of the examiner's taking of Official Notice. Note the second citation demonstrates that the method is even taught in undergraduate electrical engineering classes.

**1. The etching of silicon with XeF2 vapor**
Winters, H. F.; Coburn, J. W.
Applied Physics Letters, Volume 34, Issue 1, id. 70 (1979).
It is shown that silicon is isotropically etched by exposure to XeF2(gas) at T=300 K. Si etch rates as large as 7000 A°/min were observed for P (XeF2) <1.4×10-2 Torr and the etch rate varies linearly with P (XeF2). There was no observable etching of SiO2, Si3N4, or SiC, demonstrating an extremely large selectivity between silicon and its compounds. Therefore, thin masks constructed from silicon compounds can be used for pattern delineation. The implication of these experimental results for understanding mechanisms associated with plasma etching (including RIE) will be discussed.

**2. XeF2 Etching of Silicon** Characteristics: dry, isotropic, vapor ...
www-inst.eecs.berkeley.edu/~ee143/fa10/lab/**XeF2**_tutorial.pdf
**XeF2 etch** tutorial. Spring 2000 TAs. 1. **XeF2 Etching** of **Silicon**. Characteristics : dry, isotropic **...** Advantages of **XeF2 etching** vs. other **silicon** etchants

**Wikipedia excerpt:**

**As an etchant**

Xenon difluoride is also used as an isotropic gaseous etchant for silicon, particularly in the production of microelectromechanical systems, (MEMS). Brazzle, Dokmeci, et al., describe this process: Brazzle, J.D.; Dokmeci, M.R.; Mastrangelo, C.H.; Modeling and characterization of sacrificial polysilicon etching using vapor-phase xenon difluoride, 17th IEEE International Conference on Micro Electro Mechanical Systems (MEMS), 2004, pages 737-740.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

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**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALLAN OLSEN whose telephone number is (571)272-1441. The examiner can normally be reached on M, W and F: 1-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on 571-272-1435. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Allan Olsen/
Primary Examiner, Art Unit 1716